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Multi Objective Analysis of NCL Threshold Gates with Return To Zero Protocols

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Abstract: *This work scrutinizes the implementation and performance analysis of novel self-timed asynchronous logic. These templates are based on a delay-insensitive (DI) logic paradigm known as NULL Convention Logic (NCL) that supports RTZ protocol, includes clock-free operation, dual-rail encoding and monotonic transitions. Potential benefits include inherent robustness, low power, reduced noise ratio, easy design reuse and reduced switching activity. In this work quantitative analysis have been carried out on both conventional static CMOS approach and the proposed static NCL approach using Tanner tools and the corresponding power, delay, noise and power-delay product for both designs have been collected and compared.*
Key Words*: Low Power Design- DI-NCL-RTZ*

I. INTRODUCTION

From the last few decades, the focus of conventional digital logic design has been basically on clocked, synchronous architectures [1]. However, as clock rates increases feature size decreases, causing clock skew, a significant problem. To achieve acceptable skew, high performance chips dedicate large amount of area for clock drivers causing these chips to consume high power particularly at the clock edge. As these trend continues, the complexity in clock increases and innate power inefficiencies in clocked architectures as the dominant factor hindering efficiency of the circuit [2, 3]. These issues have evolved renewed interest in clock-less architecture so called self-timed asynchronous paradigms. When compared to clocked architectures, self-timed templates require low power, less electro-magnetic interference (EMI), and less noise without degrading the performance of the system. Furthermore, when designing intricate circuits like Systems-on-Chip (SoCs) the delay-insensitive (DI) asynchronous paradigms have added advantages like component reuse, increased robustness, mitigate clock related problems and abridged crosstalk between analog and digital paradigms. In the semiconductor industry, asynchronous paradigms will be rifer when the demand increases for templates with high performance, decreased feature size and greater intricacy as prognosticated by the International Technology Roadmap for Semiconductors (ITRS) [3, 4].

In this paper, we scrutinize novel delay insensitive asynchronous paradigm, NULL convention logic (NCL) that supports Return-to-Zero protocol. To realize self-time characteristics, NCL exploits symbolic completeness of inputs [5]. Conventional Boolean logic is symbolically input incomplete as the output is valid only when the gate is referring with time. To eradicate these time references, NCL exploits dual rail signals and quad rail signals. In this paper, we present the transistor level implementation of static NCL gates. We show that these NCL gates offers high speed operation and dissipates less power with a small increase in area when compared to standard static CMOS gates. We also show that the gates generate less noise there by achieving better performance. The rest of the paper follows as section II provides the background of NULL convention logic while section III describes the transistor level NCL topology and section IV compares NCL to conventional CMOS logic. Finally section V draws conclusions and presents areas for future exertion.

II. NULL CONVENTION LOGIC

NULL Convention Logic is a delay-insensitive self-timed logic design paradigm [5, 16]. NCL circuits attain delay insensitivity due to exploitation of dual-rail or quad-rail signals. Dual-rail logic efficiently corresponds to four states (NULL, DATA0, DATA1, and Illegal). Among these four states, three are valid states (NULL, DATA0, and DATA1) in which the control signal NULL represents no value and is exploited for self-timed handshaking, DATA0 and DATA1 corresponds to Boolean logic values 0 and 1. The last state is the illegal state where the two rails are mutually exclusive [6]. Due to complementary rails, NCL achieves uniform power consumption and further adhere to monotonic transitions between NULL and DATA wave-fronts that produce no glitch, unlike Boolean clocked architectures that generates significant glitch power. Delay-insensitive self-timed NCL systems offer better computation times, reduce switching activity and noise.

2.1. Threshold Gates

NCL threshold gates exploits hysteresis [3, 5, 7] to adhere state information, provides a means for complete switching of input signals.

NCL employs 27 primary threshold logic gates that can generate all functions of four or lesser inputs.

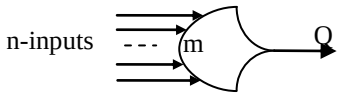

Figure 1: THmn threshold NCL gate

THmn gate is one of the primary types of threshold NCL gate with n-inputs and output, Q where the inputs are coupled to the curved part of the logic gate. The threshold, m is written in the gate, where $1 \leq m \leq n$. While THmnWw1w2…wR is another type of threshold gate, called weighted NCL threshold gate. Weighted NCL threshold gates contain an integer value, $m \geq wR > 1$, given to input R. Here $1 \leq R < n$, where n is the number of inputs, m is the threshold and w1, w2, w3 . . . wR, each greater than 1, are the input weights of 1 to R respectively [3, 8, 9].

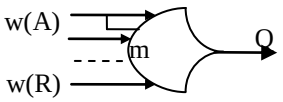

Figure 2: Weighted THmnWw1w2…wR NCL gate

2.2. Return-to-Zero Protocol

Handshake protocols are characterized into 2-phase or 4-phase protocols. When compared to 2-phase, 4-phase protocols are easier to implement and greatly reduces hardware overheads. When the 1 of n dual-rail codes are integrated to a 4-phase handshake protocol, communication starts by the sender. The valid DATA is obtained exactly when one of the n wires is at a precise DATA value and the absence of DATA, called spacer can be given by any of the (2n-n) DR codes [10].

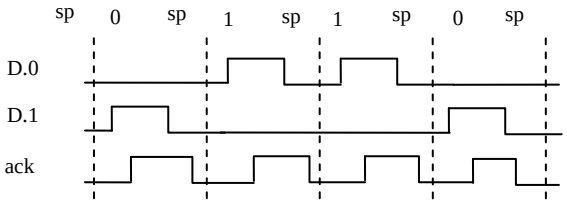

Figure 3: RTZ 1-of-2 data transmission.

TABLE I: RTZ Protocol.

Wire Name	Spacer	Bit ‘0’	Bit ‘1’
D.t	0	0	1
D.f	0	1	0

In RTZ protocol containing 1-of-2 DR codes, transmission starts when all the rails are at logic 0. When the valid DATA is encoded, it is propagated in the channel and the receiver acknowledges it with ack signal. After the propagation of valid DATA in the channel all the rails returns to zero to indicate absence of DATA, called spacer. When the spacer is acknowledged by the receiver, communication ends and transmits a new DATA in the channel [11, 12].

III. TRANSISTOR LEVEL IMPLEMENTATION OF STATIC NCL GATES

Several transistor level implementations of NCL gates were introduced that includes dynamic, semi-static [13]. The dynamic NCL does not exploit a feedback system to adhere state information, so it is not a DI. While the semi-static NCL paradigms employs feedback but the downside is the presence of week inverter that cannot sink or source adequate current to resist internal noise. To overcome these downsides in dynamic and semi-static NCL, we present the static NCL implementation. The static NCL topology exploits an additional

pull-up and pull-down networks so called Hold 0 and Hold 1 to adhere state information. The set from figure 4 represents the functionality of the gate, reset corresponds to ORing all the inputs together while Hold0 is the complement of set, i.e $\text{Hold0} = \overline{\text{set}}$ and Hold1 is the complement of reset, i.e $\text{Hold1} = \overline{\text{reset}}$ [14, 15].

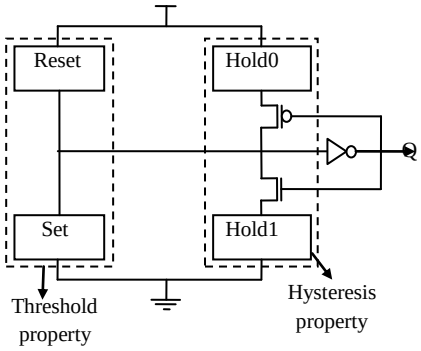

Figure 4: Static NCL gate topology

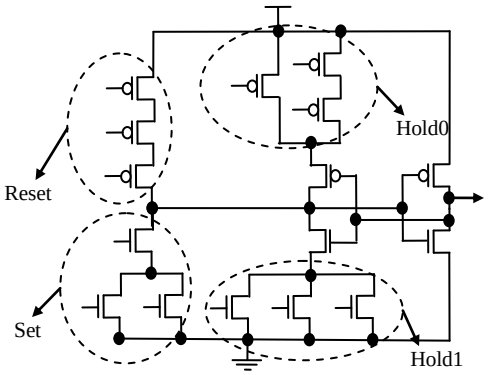

Figure 5: TH33w2 NCL gate

Figure5 shows the static implementation of TH33w2 NCL gate whose n=3 and m=3. The input A, B and C are received from alternating DATA and NULL wave-fronts. Initially assume a NULL wave-front is propagated with all the inputs of the gate being NULL. If a DATA value is given to input A it remains in NULL state since no threshold is met. When a DATA value is asserted to the second input group B or to input C, the TH33w2 gate assert the valid DATA value since it meets its threshold, m=3 as the weight of input A is 2. Thus the completeness of the input is achieved and complete DATA wave-front is propagated through the output. Thus the threshold gate insists completeness of the input DATA with respect to NULL. When one of the input DATA becomes NULL the circuit asserts DATA value due to its threshold. To assert a complete NULL wave-front all the inputs of the gate must be NULL and hence the gate switches the output to NULL ending the transition of DATA and starts a new communication. Thus the threshold gate insists completeness of input NULL with respect to DATA.

IV. RESULTS AND DISCUSSIONS

The proposed static NCL design is compared with conventional CMOS design in terms of power, system noise, propagation delay and power-delay product using Tanner tools with 250nm technology.

4.1. Power Consumption

Average power for all the 27 threshold gates are implemented using NCL and CMOS topologies and the simulated values are tabulated in table II. From the evaluated results the static NCL offers minimum power compared to conventional gates.

$$P_{avg} = P_{dynamic} + P_{static}$$

Where $P_{dynamic}$ is the total dynamic power and P_{static} is the static power of the gates [17].

Table II: Simulation results for power in CMOS and NCL designs.

GATES	CMOS	NCL
TH12	4.97×10^{-5}	6.52×10^{-5}
TH22	6.01×10^{-5}	7.60×10^{-5}
TH13	2.00×10^{-5}	2.99×10^{-5}
TH23	5.16×10^{-5}	3.18×10^{-5}
TH33	2.93×10^{-5}	3.23×10^{-5}
TH23W2	3.36×10^{-5}	3.11×10^{-5}
TH33W2	3.08×10^{-5}	3.56×10^{-5}
TH14	9.07×10^{-5}	1.42×10^{-5}
TH24	3.64×10^{-5}	2.03×10^{-5}
TH34	3.72×10^{-5}	1.70×10^{-5}
TH44	1.50×10^{-5}	1.85×10^{-5}
TH24W2	2.45×10^{-5}	1.73×10^{-5}
TH34W2	3.03×10^{-5}	1.03×10^{-5}
TH44W2	2.97×10^{-5}	1.11×10^{-5}
TH34W3	1.68×10^{-5}	1.77×10^{-5}
TH44W3	1.51×10^{-5}	1.81×10^{-5}
TH24W22	1.70×10^{-5}	1.63×10^{-5}
TH34W22	2.78×10^{-5}	2.10×10^{-5}
TH44W22	2.64×10^{-5}	1.59×10^{-5}
TH54W22	1.85×10^{-5}	2.05×10^{-5}
TH34W32	1.71×10^{-5}	1.68×10^{-5}
TH54W32	1.85×10^{-5}	1.88×10^{-5}
TH44W322	2.26×10^{-5}	1.70×10^{-5}
TH54W322	2.73×10^{-5}	1.92×10^{-5}
THxor0	4.14×10^{-5}	1.58×10^{-5}
THand0	2.83×10^{-5}	1.44×10^{-5}
TH24comp	3.30×10^{-5}	1.74×10^{-5}

4,2. System Noise

The major sources of noise in CMOS digital systems are due to supply and ground, charge leakage,glitches and charge sharing. Due to this the conventional architectures produce more and more noise. To reduce the generation of noise in the clocked Boolean architectures the proposed NCL is used that can greatly reduce the effect of noise in the digital circuits. The evaluated results of both the logic styles are simulated and tabulated in table III.

Table III: Evaluation results for system noise.

GATES	CMOS	NCL
TH12	1.70K	73.26
TH22	1.27X	73.11
TH13	1.13K	165.43
TH23	823.49K	165.28
TH33	3.50X	165.30
TH23W2	393.83K	165.51
TH33W2	196.99K	165.31
TH14	852.23	524.58
TH24	31.81K	263.10
TH34	959.17K	263.01
TH44	8.10530X	263.05
TH24W2	51.53K	262.58
TH34W2	115.81K	263.10
TH44W2	440.36K	263.08
TH34W3	715.20K	262.47
TH44W3	177.12K	263.10
TH24W22	232.86K	261.62
TH34W22	46.68K	263.10
TH44W22	1.23X	263.01
TH54W22	4.12X	263.04
TH34W32	78.76K	262.23
TH54W32	883.64K	263.07
TH44W322	106.57K	263.10
TH54W322	970.22K	263.08
THxor0	597.12K	263.03
THand0	507.28K	262.97
TH24comp	597.12K	263.03

4.3. Gate Delay

Gate delay or propagation delay is the time taken by the input signal to propagate through the output. It is given by

$$T_{pd} = \frac{(T_{phl} + T_{plh})}{2}$$

Where T_{pd} is the total propagation delay, T_{phl} is the propagation from high to low transition and T_{plh} is the propagation from low to high transition.The downside is that, from the experimental results tabulated in table IV the proposed NCL designs offers more delay than the CMOS gates.

Table IV: Propagated results for delay in both CMOS and NCL threshold gates.

GATES	CMOS	NCL
TH12	20.60n	20.79n
TH22	19.50n	20.71n
TH13	46.62n	40.81n
TH23	623.93p	40.81n
TH33	40.15n	40.45n
TH23W2	40.44n	40.78n
TH33W2	39.95n	40.83n
TH14	80.80n	80.90n
TH24	776.44p	80.93n
TH34	380.41p	80.91n
TH44	80.13n	80.87n
TH24W2	786.59p	80.93n
TH34W2	40.37n	80.91n
TH44W2	40.53n	80.90n
TH34W3	80.61n	80.92n
TH44W3	80.41n	80.88n
TH24W22	80.68n	80.93n
TH34W22	754.54p	80.92n
TH44W22	419.87p	80.91n
TH54W22	80.22n	80.86n
TH34W32	80.64n	80.92n
TH54W32	79.95n	80.90n
TH44W322	767.11p	80.92n
TH54W322	437.29p	80.91n
THxor0	245.37p	80.91n
THand0	541.27p	80.92n
TH24comp	454.20p	80.91n

4.4. Power Delay Product

The power delay product is the product of power and time of the gate to measure the system performance.
PDP=P. T
Where P is the average power and T is the total delay of the circuit.
From the simulation results the PDP is more for the proposed NCL design due to increase in delay of the circuit. To achieve better performance the delay of the NCL gates must be reduced.

Table V: Evaluation results for PDP in Conventional and Static NCL gates.

GATES	CMOS	NCL
TH12	1.02×10^{-12}	1.35×10^{-12}
TH22	1.19×10^{-12}	1.57×10^{-12}
TH13	9.32×10^{-13}	1.22×10^{-12}
TH23	3.23×10^{-14}	1.29×10^{-12}
TH33	1.17×10^{-12}	1.30×10^{-12}
TH23W2	1.35×10^{-12}	1.26×10^{-12}
TH33W2	1.23×10^{-12}	1.31×10^{-12}
TH14	7.32×10^{-13}	1.14×10^{-12}
TH24	2.60×10^{-14}	1.64×10^{-12}
TH34	1.41×10^{-14}	1.37×10^{-12}
TH44	1.20×10^{-12}	1.49×10^{-12}

TH24W2	1.92×10^{-14}	1.40×10^{-12}
TH34W2	1.22×10^{-12}	8.33×10^{-12}
TH44W2	1.20×10^{-12}	8.97×10^{-12}
TH34W3	1.35×10^{-12}	1.43×10^{-12}
TH44W3	1.21×10^{-12}	1.46×10^{-12}
TH24W22	1.37×10^{-12}	1.31×10^{-12}
TH34W22	2.09×10^{-14}	1.69×10^{-12}
TH44W22	1.10×10^{-14}	1.23×10^{-12}
TH54W22	1.48×10^{-12}	1.65×10^{-12}
TH34W32	1.37×10^{-12}	1.35×10^{-12}
TH54W32	1.47×10^{-12}	1.52×10^{-12}
TH44W322	1.73×10^{-14}	1.37×10^{-12}
TH54W322	1.19×10^{-16}	1.55×10^{-12}
THxor0	1.01×10^{-15}	1.26×10^{-12}
THand0	1.53×10^{-14}	1.16×10^{-12}
TH24comp	1.49×10^{-14}	1.40×10^{-12}

V. CONCLUSION AND FUTURE SCOPE

A delay-insensitive asynchronous static NCL design paradigms has been proposed and validated in this work. All the 27 NCL cells are implemented and its performance was analyzed in terms of PDP, delay, noise and power dissipation using Tanner EDA with 250nm technology. The static NCL gates are compared with CMOS design and from the analysis NCL generates less noise and minimum power dissipation over its traditional CMOS counter parts. The downside is it incurs delay overhead. A possible area for future work is to reduce the propagation delay to achieve better performance.

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